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10/585,696	05/18/2008	Jean Paul Petrolli	1512-90	7179

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,696	PETROLLI, JEAN PAUL	
	Examiner	Art Unit	
	SAIF A. ALHIJA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been presented for examination.

PRIORITY

2. Acknowledgment is made of applicant's claim for foreign priority based on PCT/FR05/00529 filed 7 March 2005 which claims benefit from foreign application FR 0402419 filed 8 March 2004. The Examiner notes the copy of the PCT application, however, applicant has not filed a certified copy of the FR 0402419 application as required by 35 U.S.C. 119(b).

Oath/Declaration

3. Acknowledgment is made of applicant's declaration filed 15 May 2008.

Drawings

4. Acknowledgment is made of applicant's drawings including Figures 1-18 filed 10 July 2006.

Claim Interpretation

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 1-14 are rendered statutory** by virtue of their recitation of a hardware electronic circuit as well as a corresponding hardware programmable logic array, according to paragraph 14 of the specification of the instant application.

35 U.S.C. 112 6th paragraph reads as follows:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

6. The Examiner notes that the claims recite several "means of" steps however since the claims do not expressly recite the term "means for" or "steps for" the claims will not be interpreted to invoke the 112 6th

paragraph. Applicants are respectfully advised that if they wish for there to be an invocation of 112 6th paragraph that the claims be amended to explicitly recite "means for" or "steps for."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-14 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Hoare, II et al. "Discrete Event Simulator" U.S. Patent Pub. No 2002/0133325, hereafter referred to as Hoare.**

Regarding claim 1:

The reference discloses Electronic circuit of data processing to emulate a logic function the circuit comprising:

a single clock providing representative signals of a time unit; **(Hoare. Paragraph 160, whereby the circuit timing is clocked according to its most precise and accurate representation of the simulation)**

a synchronous programmable logic array processing values per time unit; **(Hoare. Paragraph 160, whereby each circuit module which represents a circuit gate or circuit subsection synchronizes based on delays required by the circuit components. Also paragraph 98 recites that the system controls the global synchronization time of the processing elements. See also paragraph 80 reciting the use of PLDs and FPGAs to emulate circuit behavior)**

a means of state change detection designating events as internal or external values; **(Hoare. Paragraph 43 recites that the system monitors model state/value changes. The system further defines events as future or pending events which represent the internal or external events recited since the future/pending events are defined as those that are currently being simulated, interpreted as internal, and those that must be scheduled and then processed, interpreted as external)**

a means of programming signals for changing state or directly programming the events; and **(Hoare. Paragraph 86 whereby a change in one or more input signals is defined as an event which is then evaluated)**

a means of successive scheduled times processing providing a logic array with representative scheduled time signals according to the signals provided by the means of state change detection or by the means of programming signals or the events processing mean being adapted to determine scheduled times, at time delays by programming the programming means a function to happen being provided **(The Examiner notes that the phrase "to happen being provided" appears to be non-limiting as it appears to suggest or make optional the proceeding limitations, see MPEP 2106 II C. The Examiner will interpret this limitation to read without this phrase in the interests of compact prosecution pending resolution by Applicants.)** with signals by the means of detection; **(The Examiner interprets this limitation to read on scheduling time signals included in the event processing as well as the incorporation of time delays. Hoare. Paragraph 160, whereby each circuit module which represents a circuit gate or circuit subsection synchronizes based on delays required by the circuit components. Further paragraph 36 recites the use of a scheduler which accepts all future events and then sorts the events to be processed as scheduled events)**

wherein processed operations done by the logic array result from successive scheduled times initiated by internal or external state changes; and **(Hoare. Paragraph 43 recites that the system monitors model state/value changes. The system further defines events as future or pending events which represent the internal or external events recited since the future/pending events are defined as those that are currently being simulated, interpreted as internal, and those that must be scheduled and then processed, interpreted as external. Further paragraph 41 recites that the simulators keep track of pending events and when ready to be performed they are decoded, reevaluated, updating time stamps and scheduled)**

a successive scheduled time determination. **(Hoare. Paragraph 36, whereby the simulator tracks the simulation time and sends pending events based on the scheduling)**

Regarding claim 2:

The reference discloses Electronic circuit according to the claim 1, wherein the logic array reproduces a simulator operation integrated into an electronic circuit, **(Hoare. Paragraph 102 reciting hardware simulators)**

a clock defining time unit being tuned for reproduction of the simulator. **(Hoare. Paragraph 42, reciting clock cycle access to data for the simulation)**

Regarding claim 3:

The reference discloses Electronic circuit according to the claim 1, wherein the logic array is able to emulate, at real time, **(The Examiner notes that "is able to" appears to recite a capability and not a positive limitation. The Examiner notes paragraph 25 of Hoare which shows that the invention can run at various speeds and even up to faster than real time which reads on this limitation)** a logic function without any logic element emulation**. (Hoare. Paragraph 19, whereby the functional logic simulation is broken up into two parts, the logic based and the timing based. The timing propagation simulation represents non-logic element emulation.)**

Regarding claim 4:

The reference discloses Electronic circuit according to Claim 1, wherein the logic array is comprised of internal logic processing cells and peripheral communication cells with the outside of the electronic circuit, the signals provided by the scheduled time processing controlling the operation through at least one internal cell or one peripheral cell. **(Hoare. Paragraph 64 whereby the simulation engines are peripherally connected to the scheduler, element 110, and host workstation of Figure 1. The engines, scheduler and workstation represent groups of cells of processing and are contained in the modules in the reference)**

Regarding claim 5:

The reference discloses Electronic circuit according the claim 4, wherein the cells exchange data through one single group of lines on which is set up an exchange per time unit **(Hoare. Figure 1, element 107 whereby each simulation engine module, communicates through its single line group. Further paragraph 42 recites single clock cycle access to a block of stored data.)** , the cells being adapted to generate signals, random or programmed events, towards the scheduled time processing unit, the means of processing scheduled time providing to each cell a command group.**(Hoare. The scheduler, element 110, represents the scheduled time processing unit and host workstation of Figure 1 provides a user interface for interaction. The simulation engines, elements 105, deal with the signaling for the events. The command group is represented by the scheduler which allocates events as required by timing)**

Regarding claim 6:

The reference discloses Electronic circuit according to Claim 4, wherein the cells of internal processing cells are able to process a logic word per time unit. **(Paragraph 42, recites single clock cycle access to a block of data and its corresponding command, such as read/write, which reads on the logic word per time unit whereby logic words are represented as read/write or other events. This is further stated in paragraph 85 whereby a read/write operation is performed in either a single clock cycle or multiple clock cycles depending on the size of the operation and its corresponding data)**

Regarding claim 7:

The reference discloses Electronic circuit according to claim 6, wherein the internal logic cells are adapted to merge several data group issued of several respective identities and to memorize each merged logic word. **(Paragraph 37 recites that the simulation engine allows for multiple pending events, such as read/writes, to be evaluated within one or more clock cycles. Paragraph 16 recites the storage of data as it is being evaluated for scheduling which reads on the memorizing of a merged logic word in that multiple operations are performed in a single cycle and the operations are based on the scheduler "memorizing" by storing the appropriate event and its relevant data)**

Regarding claim 8:

The reference discloses Electronic circuit according to Claim 4, wherein the peripheral cells are adapted to sample logic words received from the external of the circuit and to generate merged logic words according the communication direction. **(As recited above Paragraph 37 recites that the simulation engine allows for multiple pending event execution. Paragraph 16 recites the storage of data as it is being evaluated for scheduling and further the read/write recitation reads on the communication direction in that a read operation brings data into the scheduled event and the write operation sends the scheduled event data result out.)**

Regarding claim 9:

The reference discloses Electronic circuit according to the claim 5, wherein the logic array is comprised of a specific means of communication with the outside of the circuit, the logic array setting up memorized logic words adapted to be read or modified by the specific communication mean. **(As recited above Paragraph 16 recites the storage of data as it is being evaluated for scheduling and further the read/write recitation reads on the communication means in that a read operation communicates data into the scheduled event and the write operation communicates the scheduled event data result out.)**

Regarding claim 10:

The reference discloses Simulator comprising: an electronic circuit according to Claim 1. **(Examiner note: This claim is being interpreted as an independent claim incorporating the limitations of claim 1. Paragraph 9 reciting the types of discrete event simulators)**

Regarding claim 11:

The reference discloses Emulator comprising: an electronic circuit according to Claim 1. **(Examiner note: This claim is being interpreted as an independent claim incorporating the limitations of claim 1. Paragraph 9 reciting hardware and software emulated cores as types of discrete event simulators)**

Regarding claim 12:

The reference discloses Electronic circuit according the claim 4, further comprising: a scheduler needing no scheduled time processing other than delays managed by a register matrix and a conflict detection between scheduled times. **(Hoare. Paragraph 126 whereby the scheduler keeps events in order and prevents conflict based on the calculated delay and further the delaying register matrix is seen in Figure 13b as the elements D1 through D4, which are delay components holding the data until appropriate to continue by using data registers thereby delaying the outputs of E1 through E4.)**

Regarding claim 13:

The reference discloses Electronic circuit according the claim 12, wherein the specific communication means reads and changes scheduled times. **(Hoare. Paragraph 126 whereby the scheduler keeps events in order based on the calculated delay in order to prevent conflict.)**

Regarding claim 14:

The reference discloses Electronic circuit according the claim 4, further comprising: a logic combination of output datas formed of internal or peripheral communication cells. **(Hoare. Figure 1, the data communication between the differing modules, 105, 110, and the buses or communications lines, 120, 107, 115 whereby the modules contain their respective communication cells connecting to the buses or communication lines)**

Conclusion

8. All Claims are rejected.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. *Informal or draft communication, please label PROPOSED or DRAFT*, can be additionally sent to the Examiners fax phone number, (571) 273-8635.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

September 22, 2010

/Saif A Alhija/

Examiner, Art Unit 2128